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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,931	09/19/2003	Keiko Motokawa	16869S-094900US	6823

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EXAMINER	
FRANCIS, MARK P	
ART UNIT	PAPER NUMBER
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/665,931	MOTOKAWA ET AL.	
	Examiner	Art Unit	
	Mark P. Francis	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/01/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on September 19, 2003.

2. Claims 1-19 have been examined.

Oath/Declaration

3. The Office acknowledges receipt of a properly signed oath/declaration filed September 19, 2003.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1-8 and 9-18 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Regarding claims 1 and 4,

Applicant merely defines a compiler for producing an object program used to be executed on an architecture equipped with a plurality of memory hierarchies from a source program that comprises a series of software implemented steps that do not necessarily require the use of hardware. Thus, the claim as a whole can be implemented using software means only and does not result in a tangible practical application.

Regarding claim 7,

Applicant defines a compiler that interprets either an option or a delegation statement designating which memory hierarchy that the target program mainly refers to the claim as a whole can be implemented using software means only and does not result in a tangible practical application.

Thus, the claim as a whole can be implemented using software means only and does not result in a tangible practical application under 35 U.S.C. 101.

The rejection of the base claim is incorporated into their dependent claims.

Regarding claim 9,

In this instance, the language of the claim raises a question as to whether the claim is directed merely to an abstract idea that is not tied to an environment or machine which would result in a practical application that would produce a useful, concrete, and tangible result to form the basis of statutory subject matter under 35 USC 101.

According to the 101 Interim Guidelines, The tangible requirement does not necessarily mean that a claim must either be tied to a particular machine or apparatus or must operate to change articles or materials to a different state or thing. However, the tangible requirement does require that the claim must recite more than a § 101 judicial exception, in that the process claim must set forth a practical application of that § 101 judicial exception to produce a real-world result. Benson, 409 U.S. at 71-72, 175 USPQ at 676-77 (invention ineligible because had "no substantial practical application."). "[An

application of a law of nature or mathematical formula to a ... process may well be deserving of patent protection." Diehr, 450 U.S. at 187, 209 USPQ at 8 (emphasis added); see also 21 Corning, 56 U.S. (15 How.) at 268, 14 L.Ed. 683 ("It is for the discovery or invention of some practical method or means of producing a beneficial result or effect, that a patent is granted . . ."). In other words, the opposite meaning of "tangible" is "abstract."

Applicant merely defines a method for producing an object program that is used to be executed with a plurality of memory hierarchies of a source program. Although applicant states in the preamble "a method for producing an object program...", the body of the claim consists of a series of software implemented steps that do not produce a tangible result.

The rejection of the base claim is incorporated into their dependent claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

7. A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Henry. (U.S. Pat 7,000,227)

Independent claims

With respect to claims 1,4 and 7, Henry discloses an object program producing method executed by both a computer system and a compiler(Col 6:15-30, "...includes a conventional compiler...") for producing an object program used to be executed on an architecture equipped with a plurality of memory hierarchies from a source program in conjunction with a computer system,(Col 4:5-27, "...iterative optimizer...") said method comprising: a step for interpreting either an option or a designation statement designating which memory hierarchy a target program mainly refers to data present in, (Col 6:27-40, '...may also specify initial memory assignments for the routine variables...")when the target program is executed; (Col 7:34-45, "...to the intermediate code representation of the source language routine...")and a step for performing an optimizing process directed to said designated memory hierarchy.(Col 6:30-55, "...as initialize the cache...")

With respect to claim 9, Henry discloses A method for producing an object program used to be executed on an architecture equipped with a plurality of memory hierarchies from a source program in conjunction with a computer system, (Col 4:5-27, "...iterative optimizer...") wherein: said computer system executes: a step for analyzing a designation statement designating which hierarchy an object program mainly refers to

data stored in a memory of, when said object program is executed; (Col 6:27-40, "...may also specify initial memory assignments for the routine variables...")
and a step in which an optimizing process including different processes sequences according to said plural memory hierarchies is carried out with respect to said source program, (Col 6:27-40, "...may also specify initial memory assignments for the routine variables...") and an object program which has been optimized as to an access to said memory hierarchy is produced by selecting a processes sequence corresponding to the memory hierarchy designated by said designation statement. (Col 7:20-40, '...a new optimization is preferably selected according to at least one ...")

With respect to claim 19, Henry discloses An apparatus for producing an object program used to be executed on an architecture equipped with a plurality of memory hierarchies from a source program, comprising: a storage apparatus for previously storing thereinto an optimizing process containing different processes sequences according to said plurality of memory hierarchies; (Col 7:20-40, '...a new optimization is preferably selected according to at least one ...")

an input apparatus for inputting said source program and a designation statement designating which memory hierarchy an object program mainly refers to data present in, when said object program is executed;9Col 5:43-60, "...A user of the present invention inputs into a computing system...")

a processing apparatus for producing an optimized object program based upon both source program and said designation statement; (Col 7:20-50, "...a code optimizing routine makes a code optimizing change...")

and an output apparatus for outputting said optimized object program; (Col 9:12-30, "...a computing system is preferably identical...")

wherein: said processing apparatus executes: a step for analyzing said designation statement; (Col 6:35-50, "...a user supplied measuring routine for specifying a measurable characteristic...")

a step for producing an object program which has been optimized as to an access to said memory hierarchy by selecting a processes sequence corresponding to the memory hierarchy designated by said designation statement; (Col 6:40-55, "...A most optimized version...")

and a step for outputting said optimized object program form said output apparatus. (Col 9:12-30, "...a computing system is preferably identical...")

Dependent claims

With respect to claims 2 and 5, the rejection of claims 1 and 4 are incorporated respectively and further, Henry discloses that: as said optimizing process directed to the designated memory hierarchy, a memory latency is calculated according to the designated memory hierarchy with respect to an instruction for accessing a memory; and an optimizing process responding to the calculated latency is carried out. (Col 6:53-67, "...memory utilization, and execution time,...")

With respect to claims 3,6,14, and 18, the rejection of claims 1,4,9 and 14 are incorporated respectively and further, Henry discloses an object program producing method as claimed in claim 9, wherein: said optimizing process contains at least one of an optimizing process by instruction scheduling, a prefetch optimizing process, and an optimizing process by loop tiling and loop interchange/loop unrolling. (Col 6:35-67, "...a number of loop iterations...loop should not be unrolled...")

With respect to claim 8, the rejection of claim 1 is incorporated and further, Henry discloses a storage medium wherein: said storage medium has stored thereinto the compiler recited in claim 1. (Col 6:20-27, "...a conventional compiler...")

With respect to claim 10, the rejection of claim 9 is incorporated and further, Henry discloses that: said designation statement is described in an option within a compiler initiating command. (Col 6:53-67, "...a user supplied measuring routine for specifying a measurable...")

With respect to claim 11, the rejection of claim 9 is incorporated and further, Henry discloses that: said designation statement is inserted into said source program. (Col 7:20-40, "...a user provides to the code optimization software,...")

With respect to claim 12, the rejection of claim 11 is incorporated and further, Henry

discloses that: said designation statement is applied to each of plural loops contained in said source program; said analysis step includes a step for forming a loop table indicative of a correspondence relationship between the respective loops and the memory hierarchies designated by the designation statements corresponding to said loops; and said execution step includes a step for acquiring a memory hierarchy designated by said designation statement by referring to said loop table. (Col 6:25-55, "...A low number value may indicate that the most optimized...")

With respect to claim 13, the rejection of claim 9 is incorporated and further, Henry discloses that: said memory hierarchies include a hierarchy constructed of a primary cache, a hierarchy constructed of a secondary cache, and a hierarchy constructed of a main storage apparatus. (Col 5:30-50, "...common baseline cache...system/cache memory...")

With respect to claim 15, the rejection of claim 14 is incorporated and further, Henry discloses that: said optimizing process corresponds to the optimizing process by the instruction scheduling; and a number of memory access latency cycles to be set are different from each other according to said memory hierarchies in said processes sequence. (Col 5:30-50, "...common baseline cache...system/cache memory...")

With respect to claim 16, the rejection of claim 14 is incorporated and further, Henry discloses that: said optimizing process corresponds to the prefetch optimizing process;

and timing of a prefetch code to be inserted is different from each other according to said memory hierarchies in said processes sequence. (Col 7:45-67, "...if key memory prefetches in different places,...")

With respect to claim 17, the rejection of claim 14 is incorporated and further, Henry discloses that: said optimizing process corresponds to the optimizing process by the loop tiling; a tile size is different from each other according to said memory hierarchies in said processes sequence. (Col 6:35-67, "...a number of loop iterations...loop should not be unrolled...")

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark P. Francis whose telephone number is (571) 272-7956. The examiner can normally be reached on Mon-Fri 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mark P. Francis
Patent Examiner
Art Unit 2193

Primary Examiner
1-22-2007